Amendments to the Claims

1-30. (Cancelled)

31. (New) A system comprising:

an active host; and

a standby host coupled with the active host via a plurality of buses, wherein the active host and the standby host each include a controller, the controller having

a fault detection module coupled with fault detection hardware, the fault detection module to receive a notification from the fault detection hardware indicating a fault,

a bus arbiter control module to provide bus arbitration on the plurality of buses, and to coordinate control of the plurality of buses between the active host and the standby host, and

a host control (HC) interface unit to generate control signals transmitted during startup and fail-over.

32. (New) The system of claim 31, wherein the controller further comprises:

an interface to provide the controller with access to programs running on the active host and the standby host;

a Peripheral Component Interconnect (PCI)-to-PCI (P2P) control module;

a power and reset control module; and

a clock control module to provide clock signals to the plurality of buses.

33. (New) The system of claim 31, wherein the plurality of buses comprises a plurality of COMPACTPCI buses.

34. (New) The system of claim 31 to use a Redundant System Slot (RSS) architecture.

35. (New) The system of claim 32, wherein the active host and the standby host each include a plurality communication modules, and an Ethernet link coupled with the plurality of communication modules to maintain synchronization between the active host and the standby host.

36. (New) The system of claim 31, wherein the HC interface unit is further to:
receive control signals transmitted during startup and fail-over; and
respond to control signals transmitted during startup and fail-over.

37. (New) A method comprising:
receiving a notification from fault hardware indicating a fault;
providing bus arbitration on a plurality of buses;
coordinating control of the plurality of buses between an active host and a standby host; and
generating control signals to be transmitted during startup and fail-over.

38. (New) The method of claim 37, further comprising:
accessing programs running on the active host and the standby host; and
providing clock signals to the plurality of buses.

39. (New) The method of claim 37, wherein the plurality of buses comprises a plurality of COMPACTPCI buses.

40. (New) The method of claim 38, further comprising maintaining synchronization between the active host and the standby host via an Ethernet link.

41. (New) The method of claim 37, further comprising:
receiving the control signals to be used during startup and fail-over; and
responding to the control signals received during startup and fail-over.

42. (New) A method comprising:
requesting a map of bus devices from an active host;
determining whether the active host is to request split mode, wherein if the split mode is not requested, the active host is to receive a coherent bus device map; and
placing a plurality of high availability (HA) aware device drivers into a pending start state.

43. (New) The method of claim 42, further comprising:
requesting the split mode; and
determining whether the split mode request is successful, wherein if the request is successful, starting the plurality of HA aware device drivers on an adjacent bus segment.

44. (New) The method of claim 43, further comprising:

receiving an unsuccessful split mode request;

transitioning the active host to cluster mode;

loading backplane device drivers; and

starting the backplane device drivers.

45. (New) A controller comprising:

a fault detection module coupled with fault detection hardware, the fault detection module to receive a notification from the fault detection hardware indicating a fault;

a bus arbiter control module to provide bus arbitration on a plurality of buses, and to coordinate control of the plurality of buses between an active host and a standby host; and

a host control (HC) interface unit to generate control signals transmitted during startup and fail-over.

46. (New) The controller of claim 45, wherein the controller further comprises:

an interface to provide the controller with access to programs running on the active host and the standby host;

a Peripheral Component Interconnect (PCI)-to-PCI (P2P) control module;

a power and reset control module; and

a clock control module to provide clock signals to the plurality of buses.

47. (New) The controller of claim 45, wherein the plurality of buses comprises a plurality of COMPACTPCI buses.

48. (New) The controller of claim 45 to use a Redundant System Slot (RSS) architecture.

49. (New) The system of claim 45, wherein the HC interface unit is further to:
receive control signals transmitted during startup and fail-over; and
respond to control signals transmitted during startup and fail-over.